IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Previously presented) A semiconductor device structure, comprising:
a substrate including at least one recess formed therein; and
a material layer disposed over the substrate and substantially filling the at least one recess, the material layer having a substantially planar surface, portions of the material layer that cover a surface of the substrate having a thickness of less than about half a depth of the at least one recess.

2. (Canceled)

3. (Previously presented) The semiconductor device structure of claim 1, wherein the material layer comprises a mask material.

4. (Previously presented) The semiconductor device structure of claim 3, further comprising at least one conductively doped region continuous with a surface of the semiconductor substrate and adjacent the at least one recess.

5-10. (Canceled)

11. (Previously presented) The semiconductor device structure of claim 1, wherein the substrate comprises a stacked capacitor structure and the at least one recess comprises at least one container recessed in an insulator layer of the stacked capacitor structure.

12. (Previously presented) The semiconductor device structure of claim 11, wherein the material layer comprises a mask material, the mask material substantially filling the at least one container.

13-14. (Canceled)

15. (Previously presented) A semiconductor device structure, comprising:

a substrate including at least one recess formed therein;

an intermediate layer substantially filling the at least one recess and covering a surface of the semiconductor device substrate, the intermediate layer including at least one valley located substantially above the at least one recess; and

a material layer disposed over the intermediate layer and substantially filling the at least one valley, the material layer having a substantially planar surface, portions of the material layer that cover a surface of the intermediate layer having a thickness of less than about half a depth of the at least one valley.

16. (Previously presented) The semiconductor device structure of claim 15, wherein at least one region of the substrate is exposed through the material layer.

17. (Canceled)

18. (Previously presented) The semiconductor device structure of claim 15, wherein at least one region of the at least one intermediate layer is exposed through the material layer.

19. (Previously presented The semiconductor device structure of claim 15, wherein the at least one intermediate layer comprises at least one of a mask material, an insulative material, and a conductive material.

20. (Previously presented) The semiconductor device structure of claim 15, wherein the material layer has a thickness that is less than a depth of the at least one recess.

21. (Previously presented) The semiconductor device structure of claim 1, wherein the surface of the material layer is free of abrasive-planarization-induced defects.

22. (Canceled)

23. (Previously presented) The semiconductor device structure of claim 15, wherein the surface of the material layer is free of abrasive-planarization-induced defects.

24. (Canceled)

25. (Previously presented)The semiconductor device structure of claim 15, wherein the intermediate layer includes a nonplanar upper surface with at least one peak located substantially above the surface of the semiconductor device substrate and at least one valley located substantially above the at least one recess.

26. (Previously presented)The semiconductor device structure of claim 15, wherein the material layer comprises a mask layer.

27. (Previously presented)The semiconductor device structure of claim 15, wherein the material layer comprises a stress buffer layer.

28. (Previously presented) A semiconductor device structure, comprising:
a substrate including at least one recess formed therein;
an intermediate layer filling a portion of the at least one recess; and
a material layer disposed over the intermediate layer and substantially filling a remaining portion of the at least one recess, the material layer having a substantially planar surface, the material layer covering a surface of the intermediate layer having a thickness of less than about half a depth of the remaining portion of the at least one recess.

29. (Previously presented) The semiconductor device structure of claim 28, wherein the substrate includes at least one peak.

30. (Previously presented) The semiconductor device structure of claim 29, wherein the at least one peak is exposed through the intermediate layer.

31. (Previously presented) The semiconductor device structure of claim 29, wherein the at least one peak is exposed through the material layer.

32. (Previously presented) The semiconductor device structure of claim 29, wherein the at least one peak of the intermediate layer is exposed through the material layer

33. (Previously presented)A semiconductor device structure, comprising:

a substrate including at least one recess formed therein;

an intermediate layer at least partially filling the at least one recess and covering a surface of the semiconductor device substrate, the intermediate layer including at least one valley located substantially above the at least one recess; and

a material layer disposed over the intermediate layer and substantially filling the at least one valley, the material layer having a substantially planar surface, the material layer covering a surface of the intermediate layer having a thickness of less than about half a depth of the at least one valley.

34. (Previously presented)The semiconductor device structure of claim 33, wherein the at least one valley is located at least partially in the at least one recess.